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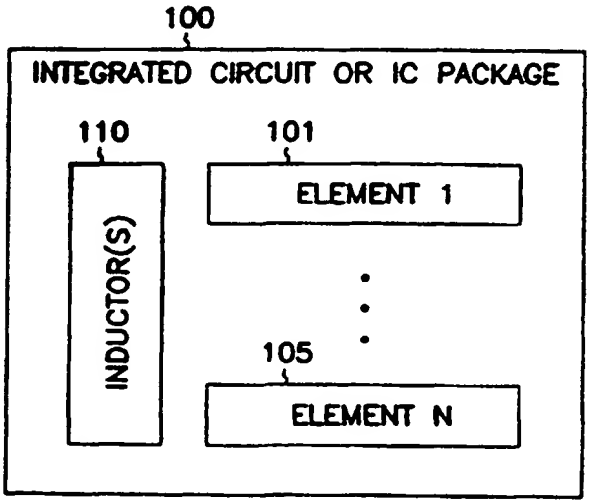
(54) Title: INDUCTOR ON INTEGRATED CIRCUIT AND METHODS FOR MANUFACTURE



(57) Abstract: An inductor (1) for an integrated circuit or integrated circuit package comprises a three-dimensional structure. In one embodiment the inductor is arranged on an integrated circuit substrate in at least two rows (2, 3), each row comprising upper segments (32) and lower segments (34), with the upper segments being longer than the lower segments. The upper segments in a first row are offset 180 degrees from those in an adjoining row to provide greater coupling of magnetic flux. The materials and geometry are optimized to provide a low resistance inductor for use in high performance integrated circuits. In another embodiment the inductor is arranged on an integrated circuit package substrate. Also described are methods of fabricating the inductor on an integrated circuit or as part of an integrated circuit package.

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INDUCTOR ON INTEGRATED CIRCUIT AND METHOD FOR MANUFACTURE

Technical Field of the Invention

The invention relates to the structure and fabrication of electrical inductors and, in particular, to an inductor forming an integral part of an integrated circuit, such as a microprocessor, or forming an integral part of an integrated circuit package.

Background of the Invention

In the field of microelectronic circuits there is an incessant competitive pressure among manufacturers to drive the performance of their circuits up while driving down production costs. This is particularly true in the field of microprocessors, where each generation of devices is expected to provide greater performance than its predecessor, to operate at increasingly higher clock speeds and increasingly lower supply voltages, and to be fabricated as cheaply as possible.

Microprocessors currently being designed will require in excess of 100 watts of power to operate, and they will operate at supply voltages of about 1 volt, so the resulting current flowing through them will be nearly 100 amps.

At the same time that the speed and power requirements of commercially competitive microelectronic circuits are constantly increasing, there is an increasingly significant need to provide passive electrical devices such as inductors and transformers directly on such circuits or as part of the integrated circuit package. Due to the high operational current expected in these devices, it is important that they be relatively low in resistance in addition to being small in size and relatively inexpensive to fabricate.

Low resistance inductors and transformers are needed in numerous microelectronic applications, such as high frequency circuits, amplifiers, circuits for reducing electromagnetic interference (EMI), power converters (including

direct-current to direct-current, alternating-current to alternating-current, direct-current to alternating current, and alternating-current to direct-current converters) for the distribution of power to circuits, and clocking circuits. In addition, other applications include radio frequency (RF) circuits such as are used in a myriad of wireless devices like cellular telephones, wireless modems, and other types of communications equipment.

Various integrated circuit inductors are known in the semiconductor art. For example, the following patents were found in the course of a search for art relating to the inventions described herein: U.S. Pat. Nos. 5,095,357, 5,635,892, 5,801,100, 5,877,533, all of which disclose various types of integrated circuit inductor structures. However, none of the known integrated circuit inductors are suitable for use in commercially competitive, high performance, low cost microcircuits, where the requirement is for low resistance, functionally effective, and relatively uncomplicated structures and processes. Some of the inductor structures disclosed in the above-mentioned patents are formed in a planar, spiral pattern, a disadvantage of which is that the magnetic flux goes down into the integrated circuit structure, causing the generation of mirror currents which can harm other circuit components.

For the reasons stated above, there is a substantial need in the semiconductor art for an inductive element for an integrated circuit and for an integrated circuit package, and method of fabrication thereof, which have relatively low resistance and which are relatively inexpensive to manufacture.

In addition, there is a substantial need in the semiconductor art for an integrated circuit and for an integrated circuit package having one or more inductive elements which have relatively low resistance and which are relatively inexpensive to manufacture.

Summary of the Invention

Accordingly, in one embodiment an integrated circuit component is described which includes a substrate and at least one multi-level inductive element.

In another embodiment, an integrated circuit is described that includes an inductive element. The integrated circuit includes a substrate and at least one multi-level inductive element.

In a further embodiment, an inductive element is described that is formed as part of an electronic package comprising an integrated circuit and a substrate.

In yet other embodiments, methods of fabricating an inductive element on an integrated circuit or integrated circuit package are described. These methods include forming a first dielectric layer in a manner that varies in the Z-dimension, and forming a first conductive layer over the first dielectric layer. The first conductive layer also varies in the Z-dimension. The first conductive layer has a length and a width, the length being substantially greater than the width in one embodiment, and the length being less than or equal to the width in another embodiment. The first conductive layer is arranged in a substantially straight line along the X-dimension.

Brief Description of Drawings

FIG. 1 illustrates a perspective, cross-sectional view of an inductive element in accordance with one embodiment of the invention;

FIG. 2 illustrates a top view of an inductive element in accordance with another embodiment of the invention;

FIG. 3 illustrates a simplified block diagram of an integrated circuit or integrated circuit package comprising an inductive element in accordance with other embodiments of the invention;

FIG. 4 illustrates a cross-sectional view of an inductive element in accordance with an embodiment of the invention in which multiple conductive layers are interconnected by vias of conductive material;

FIG. 5 illustrates a cross-sectional view of an inductive element in accordance with an embodiment of the invention in which a single conductive layer is arranged in a stepped or crenellated manner;

FIG. 6 illustrates a cross-sectional view of an inductive element in accordance with an embodiment of the invention in which a single conductive layer is arranged in an undulating manner; and

FIG. 7 illustrates a flow diagram of a method for fabricating an inductive element in accordance with one embodiment of the present invention.

Detailed Description

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

FIG. 1 illustrates a perspective, cross-sectional view of an inductive element 1 in accordance with one embodiment of the invention. In one embodiment, inductive element 1 comprises a first row 2 of a multi-layered structure and a second row 3 of a multi-layered structure. The multi-layered structure can be either an integrated circuit structure or an integrated circuit package structure.

Inductive element 1 may alternatively be fabricated with more or fewer than two rows, depending upon the functional requirements of the particular circuit or circuit package for which the inductive element is used.

By deploying the conductive element in rows, rather than in a spiral, the conductive element can be fabricated relatively wide in order to keep its electrical resistance relatively low. Given the space limitation of an integrated circuit or of a high-density integrated package, it would difficult if not

impossible to arrange a conductive element of equivalent width in a spiral pattern so as to provide the equivalent inductance with low electrical resistance.

In one embodiment, as shown in FIG. 1, the inductor is arranged on the substrate in two rows 2 and 3, with each row comprising a plurality of upper segments 32 and a plurality of lower segments 34. In one embodiment, the upper segments 32 are relatively longer than the lower segments 34. In other embodiments the relative lengths of the upper segments 32 and lower segments 34 may be different, depending upon the operational and layout requirements of the particular integrated circuit or integrated circuit package.

As seen with reference to X-Y-Z coordinate set 50 in FIG. 1, the inductor structure, comprising conductive layer 20 and magnetic layers 19 and 21, varies in the Z-dimension along rows 2 and 3.

It will also be seen in FIG. 1 that the length of the inductor structure of a given row is substantially greater than its width, and that the conductive layer in any row is arranged in a substantially straight line along the X-dimension.

In one embodiment, the upper segments 32 in a first row 2 are staggered or offset 180 degrees from those in an adjoining row 3 to provide greater coupling of magnetic flux. The offset of the upper segments 32 of row 2 by 180 degrees relative to those of adjacent row 3 provides relatively greater magnetic flux linkage between these adjacent rows. The offset between upper segments 32 in adjacent rows may be different from 180 degrees, depending upon the operational and layout requirements of the particular integrated circuit or integrated circuit package.

In the embodiment shown in FIG. 1, row 2 is coupled to row 3 using interconnect portion 40. Interconnect portion can comprise a pedestal structure between rows 2 and 3, or other suitable structures can be utilized. To minimize the resistance of inductive element 1, the length of interconnect portion 40 is minimized to the extent possible, and the width of the conductive layer 20 is fabricated relatively wide. The width of the conductive layer 20 in interconnect portion 40 depends upon the operational and layout requirements of the

particular integrated circuit or integrated circuit package. Magnetic layers 19 and 21 could be modified or eliminated in the interconnect portion 40.

The structure and composition of a given row, for example row 3, will now be explained. Substrate 10 can be formed from suitable semiconductor materials used for the fabrication of integrated circuits, such as silicon, germanium, gallium arsenide, and similar materials. It can also be formed of a polyimide, a suitable organic material, a printed circuit board, or other dielectric material like glass, quartz, or ceramic, in a manner which will be apparent to one of ordinary skill in the art. In one embodiment silicon is used. The thickness of substrate 10 is not critical.

Insulating layers 12, 15, and 25 can be formed of a suitable insulating material such as silicon dioxide. Other insulating materials could be used, such as silicon nitride, or silicon oxynitride. Any other insulating material known in the art could be used if compatible with the particular semiconductor process being used.

Magnetic layers or magnetic films 19 and 21 can be formed of any suitable magnetic material. Pure elements or alloys comprising iron, nickel, cobalt, manganese, zinc, zirconium, tantalum, rhenium, silicon and/or certain rare earths can be used. Some alloys that can be used are nickel-iron, cobalt-zirconium-tantalum, iron-tantalum-nickel, nickel-iron-rhenium, and ferro-silicon. In one embodiment, cobalt-zirconium-tantalum is used. The integrated circuit inductive element 1 can also be fabricated without magnetic layers 19 and 21, if an inductive device providing substantially less inductance meets the particular circuit or circuit package operational requirements.

Conductive layer 20 can be formed of any suitable conductive material such as a metal like copper, aluminum, tungsten, molybdenum, titanium, gold, silver, or palladium, or an alloy thereof. Conductive layer 20 can also be formed of a metal silicide or doped polysilicon. The thickness of layer 20 is typically in the range of 1 to 15 microns. In one embodiment, conductive layer 20 is formed of copper whose thickness is approximately 1 micron and whose width is

approximately 1 millimeter. In one embodiment, the end-to-end resistance of conductive layer 20 is 8-10 milliohms. The total inductance of inductive element 1 can be more than 100 nano-Henries (nH).

The various conductive, magnetic, and insulating layers can be formed by any suitable means known in the art, such as sputtering, electro-plating, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), physical vapor deposition (PVD), and the like.

FIG. 2 illustrates a top view of an inductive element 80 in accordance with another embodiment of the invention. Inductive element 80 comprises pedestals 81 alternating with trenches 83, in a structure similar to that shown regarding row 2 or row 3 of inductive element 1 shown in FIG. 1. In the embodiment of inductive element 80 shown in FIG. 2, the width 87 of inductive element 80 is substantially equal to its length 85. This geometry serves to minimize the resistance of inductive element 80. It can be used either in an integrated circuit implementation or in an integrated circuit package implementation of the inductive element. In another embodiment, the width 87 of inductive element 80 is greater than its length 85.

While inductive element 80 is shown in FIG. 2 as comprising a single row, it can comprise two or more rows, with the length 85 of each row being substantially equal to the width 87 of each row, in order to minimize the resistance of inductive element 80. In another embodiment the width 87 of each row is greater than the length 85 of the row.

FIG. 3 illustrates a simplified block diagram of an integrated circuit or integrated circuit package 100 comprising one or more inductor(s) 110 in accordance with one embodiment of the invention. Inductor(s) 110 can be like any inductive element described previously with reference to FIGS. 1 and 2

In addition to inductor(s) 110, integrated circuit or integrated circuit package 100 comprises another element or a plurality of other elements, represented schematically by Element 1 (101) through Element N (105), which

perform various electronic functions depending upon the type of integrated circuit or integrated circuit package 100.

Elements 1 through N can comprise, for example, one or more of the following: a microprocessor or microcontroller, a memory, an application specific integrated circuit (ASIC), a digital signal processor (DSP), a radio frequency circuit, an amplifier, a power converter, an EMI or other filter, a clocking circuit, and the like.

Elements 1-N can be active and/or passive elements, depending upon the desired function(s) of integrated circuit or integrated circuit package 100. It will be apparent that, in the case where element 100 is an integrated circuit package, Elements 1-N can be mounted or otherwise incorporated into integrated circuit package 100 in any suitable manner. It will also be apparent that while integrated circuit 100 is a planar integrated circuit in one embodiment, it can be any other appropriate type of integrated circuit structure.

FIG. 4 illustrates a cross-sectional view of an inductive element in accordance with an embodiment of the invention in which multiple conductive layers 124 and 128 are interconnected by vias 126 of conductive material through insulating layer 122. Similar in overall construction and inductive function to the embodiment illustrated in FIG. 1, the structure of the embodiment shown in FIG. 3 likewise varies in the Z-dimension along the substrate 120.

Via holes 126 can be formed by any suitable process, such as ion milling, reactive ion etching, drilling, routing, punching, or otherwise making holes or slots in insulating layer 122, followed by inserting a conductive material in the holes or slots, in a manner known in the art. For the purposes of simplification, magnetic layers have not been illustrated in FIG. 4 (or in FIGS. 5 and 6, discussed below) as part of the inductive element. However, they can be used in the embodiments illustrated in FIGS. 4-6 to increase the overall inductance of the inductive element.

FIG. 5 illustrates a cross-sectional view of an inductive element in accordance with an embodiment of the invention in which a single conductive layer 144 is arranged in a stepped or crenellated manner over insulating layer 142. Similar in overall construction and inductive function to the embodiment illustrated in FIG. 1, the structure of the embodiment shown in FIG. 5 likewise varies in the Z-dimension along the substrate 140, and it can be manufactured by any of a variety of processes known in the art.

FIG. 6 illustrates a cross-sectional view of an inductive element in accordance with an embodiment of the invention in which a single conductive layer 154 is arranged in an undulating manner over insulating layer 152. Similar in overall construction and inductive function to the embodiment illustrated in FIG. 1, the structure of the embodiment shown in FIG. 6 likewise varies in the Z-dimension along the substrate 150, and it can be manufactured by any of a variety of processes known in the art.

The embodiment of an inductor using an undulating pattern shown in FIG. 5 can be expected to have less magnetic flux linkage between adjacent rows than an embodiment as illustrated in FIG. 1.

FIG. 7 illustrates a flow diagram of a method 160 for fabricating an inductive element in accordance with one embodiment of the present invention. The fabrication operations described in FIG. 6 are those that relate to the fabrication of the conductive layer of the embodiment shown in FIG. 1. Other fabrication operations for the embodiment shown in FIG. 1 will depend upon the type of integrated circuit or integrated circuit package being manufactured and will be known by those of ordinary skill in the semiconductor art.

First, the process begins in box 160. In box 162 a first dielectric layer is formed in a manner that varies in the Z-dimension. (Refer to the set of X-Y-Z coordinates 50 in FIG. 1.) In this operation, the expression "layer" is used rather loosely to refer to the multi-level dielectric structure 15 (FIG. 1), which in fact will require several semiconductor process operations to fabricate.

Next in box 164 a first conductive layer is formed over the first dielectric layer. As seen in greater detail in FIG. 1, the first conductive layer (e.g. conductive layer 20 in row 2) varies in the Z-dimension, and its length is substantially greater than its width. The first conductive layer is arranged in a substantially straight line along the X-dimension. If a one-row inductive element is being fabricated, the process skips boxes 166, 168, and 170, and it ends in block 172; however, if the inductive element comprises at least two rows, the process continues in box 166. As mentioned previously regarding operation 162, in operation 164 the expression "layer" is used rather loosely to refer to the multi-level conductor structure 20 (FIG. 1), which in fact will require several semiconductor process operations to fabricate.

In box 166 a second dielectric layer is formed in a manner that varies in the Z-dimension. The first and second dielectric layers will ordinarily be fabricated simultaneously.

Next in box 168 a second conductive layer is formed over the second dielectric layer. As seen in greater detail in FIG. 1, the second conductive layer (e.g. conductive layer 20 in row 3) varies in the Z-dimension, and its length is substantially greater than its width. The second conductive layer is arranged in a substantially straight line along the X-dimension.

In box 170 the second conductive layer is coupled to the first conductive layer in the Y-dimension. The first and second conductive layers, including the portion that couples them together, will ordinarily be fabricated simultaneously.

This portion of the fabrication process ends in block 172.

The operations of the method can be carried out in any appropriate order and need not necessarily be executed in the order described with reference to FIG. 7.

As will be understood by those of ordinary skill in the art, if one or more magnetic layers, such as magnetic layer 19 or magnetic layer 21, are to be included in the inductive element, they will be formed at suitable times in the fabrication process. For example, magnetic layer 19 can be formed on

insulating layer 12 before insulating layer 15 is formed. Magnetic layer 21 can be formed after conductor 20 and insulating layer 25 have been formed.

It will also be understood that for the fabrication of those embodiments of the invention, described above, in which the width of a row of the inductor structure is greater or equal to the length of the row, the process illustrated in FIG. 7 will be appropriately modified.

In summary, the present invention provides an inductive element which is integrable with an integrated circuit or an integrated circuit package, and a method of fabrication thereof, which has relatively low resistance and which is relatively inexpensive to manufacture.

In addition, the present invention provides an integrated circuit or an integrated circuit package having one or more inductive elements which have relatively low resistance and which are relatively inexpensive to manufacture.

Further, the present invention provides a method for fabricating an inductive element which has relatively low resistance and which is relatively inexpensive to manufacture. And the present invention also provides an integrated circuit and an integrated circuit package which are fabricated in accordance with the above-described method.

It is an important advantage of the present invention that relatively uncomplicated yet effective inductors can be manufactured on integrated circuits or integrated circuit packages, which inductors have relatively low resistance that is compatible with the functional requirements of advanced processes and high performance integrated circuits and integrated circuit packages. Thus, commercially competitive integrated circuits, such as microprocessors, and integrated circuit packages incorporating such inductors can be manufactured and marketed.

It is another advantage of the present invention that a large concentration of the magnetic flux from the conductive element does not tend to go down into the integrated circuit or integrated circuit package structure, where it could cause the generation of harmful mirror currents, but instead most of the magnetic flux

stays relatively close to the surface of the integrated circuit or integrated circuit package, particularly when the conductor 20 is relatively wide.

In addition, the placement of the upper segments 32 of one row 180 degrees relative to those of the adjacent row provides relatively greater magnetic flux linkage between adjacent rows.

The disclosed invention can be modified in numerous ways and can assume many embodiments other than the forms specifically set out and described above. For example, the inductor structure could be fabricated without any magnetic material, or with the magnetic material partially or entirely enclosed by the conductor, or with the conductor partially or entirely enclosed by the magnetic material, or with magnetic material only located above the conductor, or with magnetic material only located below the conductor, or with magnetic material only located to one side of the conductor.

The invention may be practiced with any suitable type of semiconductor process known in the art.

The present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

CLAIMS

1. An integrated circuit component comprising:
   a substrate; and
   at least one multi-level inductive element.

2. An inductive element integrable with a semiconductor integrated circuit comprising:
   a substrate; and
   at least one multi-level inductive element.

3. An inductive element as recited in claim 2 wherein the inductive element is arranged on the substrate in a three-dimensional manner.

4. An inductive element as recited in claim 2 wherein the inductive element is arranged on the substrate in a manner which varies in the Z-dimension.

5. An inductive element as recited in claim 2 wherein the inductive element is arranged on the substrate in a stepped manner.

6. An inductive element as recited in claim 2 wherein the inductive element is arranged on the substrate in an undulating manner.

7. An inductive element as recited in claim 2 wherein the inductive element is arranged on the substrate in a manner that alternates between trenches and pedestals.

8. An inductive element as recited in claim 2 wherein the inductive element is arranged on the substrate in two layers interconnected by vias which comprise conductive material.

9. An inductive element as recited in claim 2 wherein the inductive element is arranged on the substrate in a serpentine pattern comprising at least two rows.

10. An inductive element as recited in claim 9 wherein each row comprises upper segments and lower segments, and in at least one row the upper segments are longer than the lower segments.

11. An inductive element as recited in claim 10 wherein the upper segments in a first row are offset 180 degrees from those in an adjoining row.

12. An inductive element as recited in claim 2 wherein the inductive element is formed as part of an electronic package comprising the integrated circuit and the substrate.

13. An inductive element as recited in claim 2 wherein the inductive element comprises a conductive element formed of a conductive material.

14. An inductive element as recited in claim 13 wherein the conductive element comprises a low resistance material.

15. An inductive element as recited in claim 14 wherein the low resistance material is from the group consisting of copper, aluminum, tungsten, molybdenum, titanium, gold, silver, palladium, a metal silicide, and doped polysilicon.

16. An inductive element as recited in claim 2 wherein the substrate is formed from the group consisting of silicon, germanium, gallium

arsenide, polyimide, organic material, a printed circuit board, glass, quartz, and ceramic.

17. An integrated circuit component comprising:
a substrate;
at least one multi-level inductive element; and
at least one layer of magnetic material.

18. An integrated circuit component as recited in claim 17 wherein the magnetic material is from the group consisting of nickel-iron, cobalt-zirconium-tantalum, iron-tantalum-nickel, nickel-iron-rhenium, and ferro-silicon.

19. An integrated circuit component as recited in claim 17 wherein the magnetic material is from the group consisting of iron, nickel, cobalt, manganese, zinc, zirconium, tantalum, rhenium, silicon, and the rare earth elements, or is an alloy whose constituents are from the group.

20. An integrated circuit component as recited in claim 17 and further comprising a conductive element, wherein the conductive element is located above the at least one layer of magnetic material.

21. An integrated circuit component as recited in claim 17 and further comprising a conductive element, wherein the conductive element is located below the at least one layer of magnetic material.

22. An integrated circuit component as recited in claim 17 and further comprising a conductive element, wherein the conductive element is located to one side of the at least one layer of magnetic material.

23. An integrated circuit component as recited in claim 17 and further comprising a conductive element, wherein the conductive element is enclosed by the at least one layer of magnetic material.

24. An integrated circuit component as recited in claim 17 and further comprising a conductive element, wherein the at least one layer of magnetic material is enclosed by the conductive element.

25. An integrated circuit that includes an inductive element, the integrated circuit comprising:

a substrate; and

at least one multi-level inductive element.

26. A method of fabricating an inductive element on an integrated circuit comprising:

forming a first dielectric layer in a manner that varies in the Z-dimension; and

forming a first conductive layer over the first dielectric layer, the first conductive layer also varying in the Z-dimension, the first conductive layer having a length and a width, the length being substantially greater than the width, and the first conductive layer being arranged in a substantially straight line along the X-dimension.

27. A method as recited in claim 26 and further comprising:

forming a second dielectric layer in a manner that varies in the Z-dimension;

forming a second conductive layer over the second dielectric layer, the second conductive layer also varying in the Z-dimension, the second conductive layer having a length and a width, the length being substantially greater than the width, and the second conductive layer

being arranged in a substantially straight line along the X-dimension; and

coupling the second conductive layer to the first conductive layer.

28. An integrated circuit package fabricated by:

forming a substrate;

forming at least one multi-level inductive element on the substrate; and

mounting an integrated circuit on the substrate.

29. An integrated circuit component fabricated by:

forming a first dielectric layer in a manner that varies in the Z-dimension; and

forming a first conductive layer over the first dielectric layer, the first conductive layer also varying in the Z-dimension, the first conductive layer having a length and a width, the width being greater or equal to the length, and the first conductive layer being arranged in a substantially straight line along the X-dimension.

30. An integrated circuit component as recited in claim 29 and further fabricated by:

forming a second dielectric layer in a manner that varies in the Z-dimension;

forming a second conductive layer over the second dielectric layer, the second conductive layer also varying in the Z-dimension, the second conductive layer having a length and a width, the width being greater or equal to the length, and the second conductive layer being arranged in a substantially straight line along the X-dimension; and

coupling the second conductive layer to the first conductive layer in the Y-dimension.

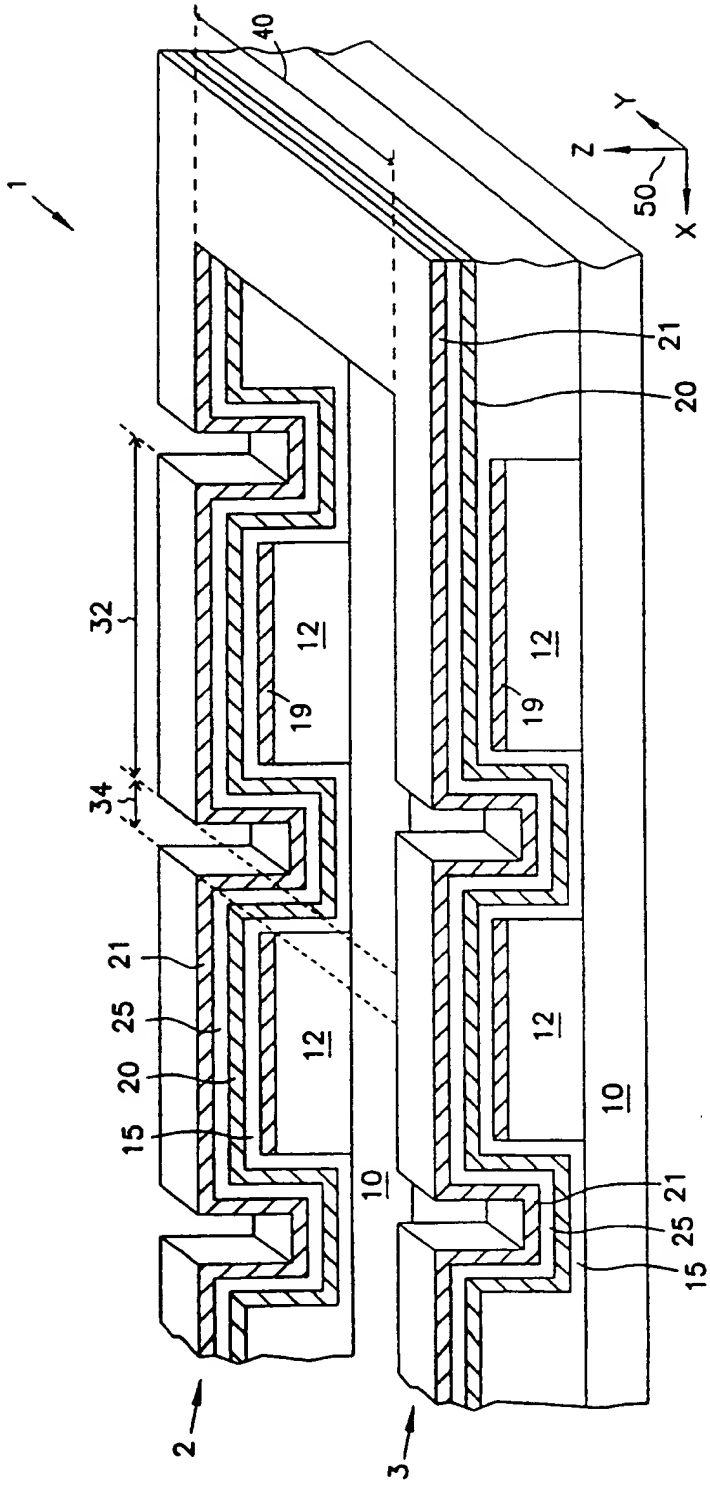

FIG. 1

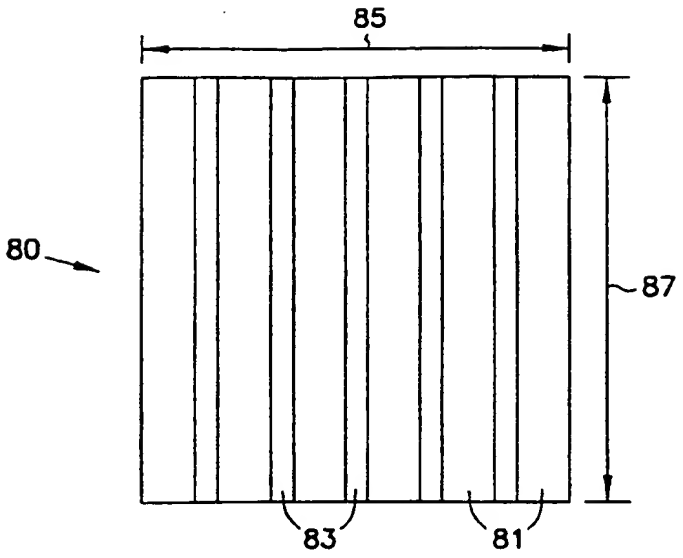
85
80
87
83
81

FIG. 2

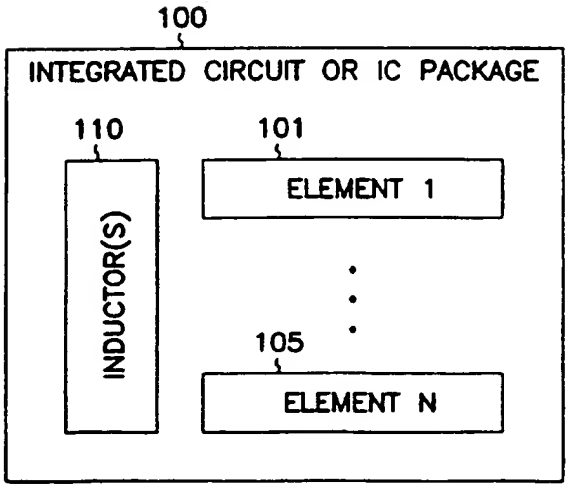
100
INTEGRATED CIRCUIT OR IC PACKAGE
110
101
INDUCTOR(S)
ELEMENT 1
105
ELEMENT N

FIG. 3

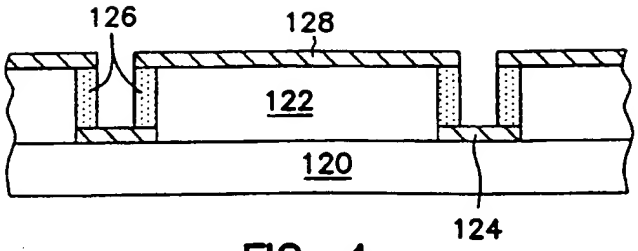

FIG. 4

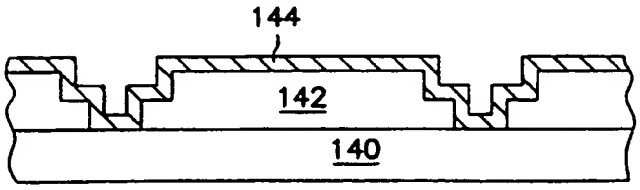

FIG. 5

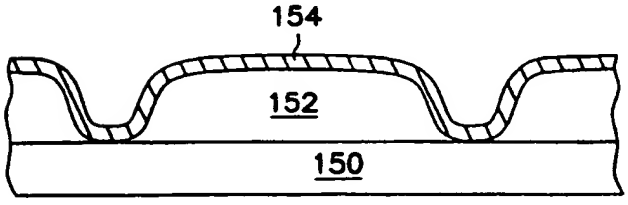

FIG. 6

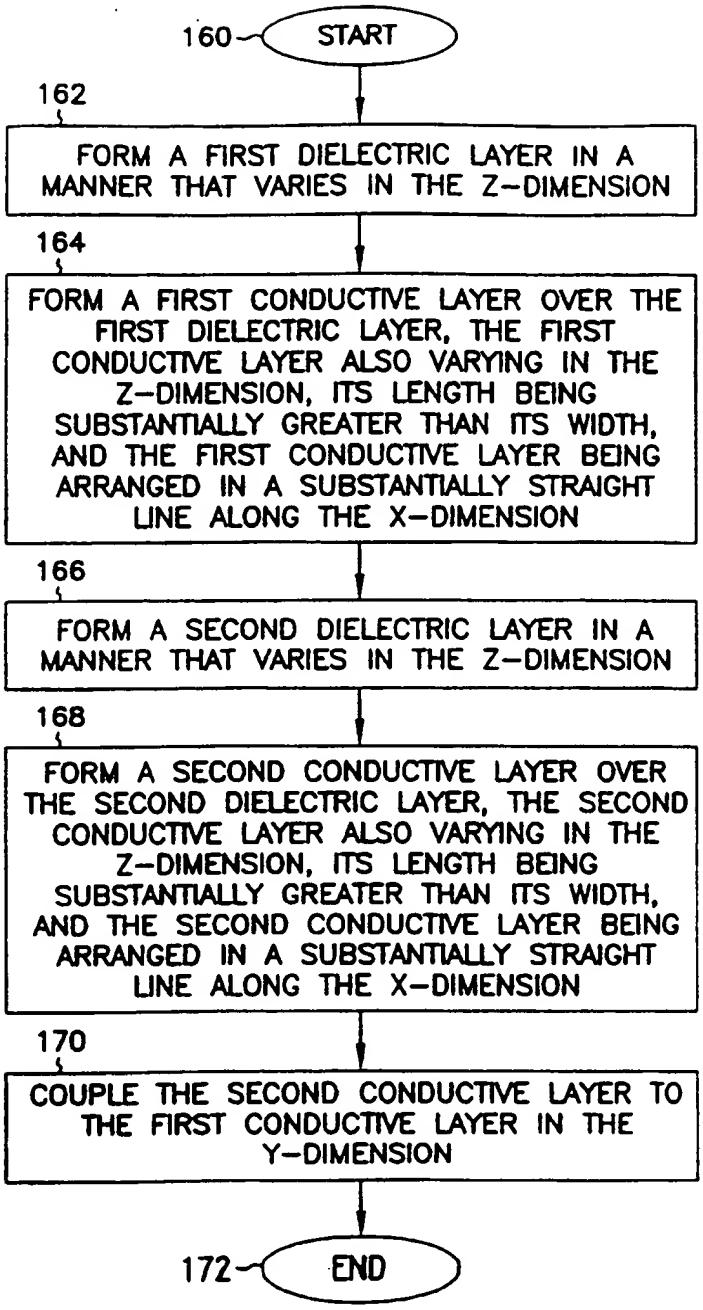
160
START
162
FORM A FIRST DIELECTRIC LAYER IN A MANNER THAT VARIES IN THE Z-DIMENSION
164
FORM A FIRST CONDUCTIVE LAYER OVER THE FIRST DIELECTRIC LAYER, THE FIRST CONDUCTIVE LAYER ALSO VARYING IN THE Z-DIMENSION, ITS LENGTH BEING SUBSTANTIALLY GREATER THAN ITS WIDTH, AND THE FIRST CONDUCTIVE LAYER BEING ARRANGED IN A SUBSTANTIALLY STRAIGHT LINE ALONG THE X-DIMENSION
166
FORM A SECOND DIELECTRIC LAYER IN A MANNER THAT VARIES IN THE Z-DIMENSION
168
FORM A SECOND CONDUCTIVE LAYER OVER THE SECOND DIELECTRIC LAYER, THE SECOND CONDUCTIVE LAYER ALSO VARYING IN THE Z-DIMENSION, ITS LENGTH BEING SUBSTANTIALLY GREATER THAN ITS WIDTH, AND THE SECOND CONDUCTIVE LAYER BEING ARRANGED IN A SUBSTANTIALLY STRAIGHT LINE ALONG THE X-DIMENSION
170
COUPLE THE SECOND CONDUCTIVE LAYER TO THE FIRST CONDUCTIVE LAYER IN THE Y-DIMENSION
172
END

FIG. 7

INTERNATIONAL SEARCH REPORT

Inte. ...nal Application No
PCT/US 00/31984

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01F17/00 H01F41/04 H01L23/64

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01F H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SHIRAKAWA K ET AL: "THIN FILM CLOTH-STRUCTURED INDUCTOR FOR MAGNETIC INTEGRATED CIRCUIT" IEEE TRANSACTIONS ON MAGNETICS,US,IEEE INC. NEW YORK, vol. 26, no. 5, 1 September 1990 (1990-09-01), pages 2262-2264, XP000150520 ISSN: 0018-9464 page 2, line 11 - line 19; figure 5 ---	1-5,7-9, 12-14, 17,20, 21,25
A	EP 0 725 407 A (IBM) 7 August 1996 (1996-08-07) column 4, line 16 -column 6, line 53; figures 2A-5E --- -/--	12-16, 18,19, 26,28,29

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 February 2001	27/02/2001

Name and mailing address of the ISA	Authorized officer
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Inter ...nal Application No
PCT/US 00/31984

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	YAMAGUCHI M ET AL: "CHARACTERISTICS OF MAGNETIC THIN-FILM INDUCTORS AT LARGE MAGNETIC FIELD" PROCEEDINGS OF THE INTERNATIONAL MAGNETICS CONFERENCE (INTERMAG),US,NEW YORK, IEEE, 18 April 1995 (1995-04-18), pages BS-1, XP000581941 ISBN: 0-7803-2606-7 figure 1 ---	20-24
X	US 3 881 244 A (KENDALL DON LESLIE) 6 May 1975 (1975-05-06)	28
A	abstract; claims; figures ---	26,29
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 02, 29 February 1996 (1996-02-29) & JP 07 272932 A (CANON INC), 20 October 1995 (1995-10-20) abstract -----	

1

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INTERNATIONAL SEARCH REPORT

information on patent family members

Inte. ...nal Application No
PCT/US 00/31984

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0725407 A	07-08-1996	JP 8250332 A	27-09-1996
US 3881244 A	06-05-1975	NONE	
JP 07272932 A	20-10-1995	NONE	